

REMARKS

The Office Action dated November 19, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. By this Amendment, claims 1-4 and 9-12 have been cancelled and claims 5 and 13 have been further amended to more particularly point out and distinctly claim the invention. No new matter has been added or amendments made that narrow the scope of any elements of any claims. Accordingly, claims 5-8 and 13-16 are pending in this application and are submitted for consideration.

Applicants acknowledge and thank the Examiner for indicating that claim 2 was allowed and that claims 3 and 4 would be allowable over the prior art if amended to be in independent form and to overcome the rejections under 35 U.S.C. § 112, second paragraph. However, by this Amendment, claims 3 and 4 have been cancelled.

Claims 3, 4, 11 and 12 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. By this Amendment, claims 3, 4, 11 and 12 have been cancelled, rendering them moot with regard to this rejection.

Claims 1 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Montrone et al. (U.S. Patent No. 4,707,800, "Montrone"). By this Amendment, claims 1 and 9 have been cancelled, rendering them moot with regard to this rejection.

Claims 5, 6, 10 and 13 were rejected under 35 U.S.C. § 102(b) as being anticipated by Licciardi et al. (U.S. Patent No. 4,905,179, "Licciardi"). In making this rejection, the Office Action took the position that Licciardi discloses all the elements of the claimed invention. By this amendment, claim 10 has been cancelled. Therefore, the rejection with regard to this claim is moot. However, Applicants respectfully submit

that claims 5, 6 and 13 recite subject matter that is neither disclosed nor suggested by Licciardi.

Applicants' amended claim 5 recites an incrementer including a plurality of half adder circuits, each adding a carry-in bit to an input bit to generate an output bit and a carry-out bit. The plurality of half adder circuits are connected in cascade in regard to the carry-in and carry-out bits. Each of the half adder circuits other than one for the least significant digit includes a transfer gate, having a data input and a data output. The transfer gate is turned on when the input bit is active. The data input directly receives the carry-in bit. A transistor, having a current channel, is connected between a power supply potential and the data output. A logic value of the power supply potential is equal to that of the carry-in bit in an inactive state and turned on when the input bit is inactive. A logic circuit generates the output bit, which is active when either the input bit or the carry-in bit is active. The carry-out bit is on the data output.

Applicants' amended claim 13 recites a decrementer including a plurality of half subtractor circuits each subtracting a borrow-in bit from an input bit to generate an output bit and a borrow-out bit. The plurality of half subtractor circuits are connected in cascade in regard to the borrow-in and borrow-out bits. Each of the half subtractor circuits other than one for the least significant digit include a transfer gate, having a data input and a data output. The transfer gate is turned on when the input bit is inactive. The data input directly receives the borrow-in bit. A transistor has a current channel connected between a power supply potential and the data output. A logic value of the power supply potential is equal to that of the borrow-in bit in an inactive state, and is turned on when the input bit being active; and a logic circuit, generating the output bit

which is active when either the input bit or the borrow-in bit is active, wherein the borrow-out bit is on the data output.

Licciardi discloses a CMOS cell for logic operations with fast carry propagation. As shown in Fig. 2, the adder includes adjacent elementary cells CEL1 and CEL2. CEL1 is used in even positions, and CEL2 is used in odd positions. In CEL2, complemented values of operands A, B are sent to the series transistors T3-T6 via inverters I11 and I12, respectively. In cells of odd positions, by complementing the inputs to the series transistors, the correct carry polarity at the output Cout ($2n + 1$) is recovered when $A=B$, without introducing additional delays in the carry propagation line.

However, as shown in Fig. 2, the adder of Licciardi has an inverter I1 located between transfer gates (T1, T2) of adjacent cells (CEL1, CEL2). Whereas, the incrementer of amended claims 5 and 13 has no circuit between transfer gates because the data input of the transfer gate directly receives a carry-in bit, as recited in amended claim 5, or directly receives the borrow-in bit, as recited in amended claim 13. Therefore, a carry bit or a borrow-in bit can propagate through transfer gates at a higher speed.

Therefore, it is respectfully submitted that the Applicants' invention, as set forth in claims 5 and 13, is not anticipated within the meaning of 35 U.S.C. § 102.

As claim 6 depends from claim 5, Applicants respectfully submit that claim 6 incorporates the patentable aspects thereof and is therefore allowable for at least the same reasons as discussed above.

Claims 7, 8, 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Licciardi et al. (U.S. Patent No. 4,905,179, "Licciardi"). In making this

rejection, the Office Action took the position that Licciardi discloses all the elements of the claimed invention, except for disclosing an inverter connected to the output of the most significant digit.

The Office Action asserted that it would have been obvious to one having ordinary skill in the art to provide an inverter connected to the output of the most significant digit since it is well known that an inverter provides an inverse or modified signal. However, Applicants note that the Office Action failed to provide any authority or reference in support of this position. Therefore, Applicants submit that this is impermissible hindsight and seasonably challenge this assertion.

Further, because claims 7 and 8 depend either directly or indirectly from claim 5, and claims 15 and 16 depend either directly or indirectly from claim 13, Applicants respectfully submit that claims 7 and 8 incorporate the patentable aspects of claim 5 and claims 15 and 16 incorporate the patentable aspects of claim 13, and are therefore allowable, for at least the same reasons as the independent claims.

Thus, it is respectfully submitted that the Applicants' invention, as set forth in claims 7, 8, 15 and 16, is not obvious within the meaning of 35 U.S.C. § 103.

In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 5-8 and 13-16, and the prompt issuance of a Notice of Allowability are respectfully solicited.

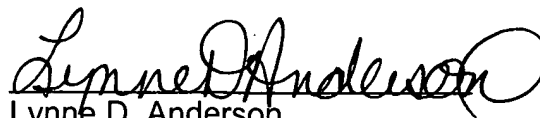
If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an

extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 107346-00020.**

Respectfully submitted,

ARENT FOX PLLC

A handwritten signature in black ink, appearing to read "Lynne D. Anderson", written over a horizontal line.

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